

U.S. Patent Application No. 10/725,776
Attorney Docket No. 351991-991290 (Formerly 2102475-991290)

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Cancelled):

Claim 2 (Currently Amended): ~~The device according to claim 1, the command buffer circuit~~
A semiconductor memory device comprising:

a memory cell array having a plurality of memory cells arranged in rows and columns, and bit lines and word lines connected to the memory cells;

a command buffer circuit, which receives at least an active signal to activate one of the rows, and a clock signal, the command buffer circuit generating an internal precharge signal to precharge the bit lines based on the active signal;

a latch circuit to which the clock signal and the active signal are supplied, the latch circuit latching the active signal in response to the clock signal;

a logic circuit to which the active signal latched by the latch circuit and the clock signal are supplied, the logic circuit generating the internal precharge signal; and

a delay circuit which delays the internal precharge signal supplied from the logic circuit, and generates an internal active signal.

Claim 3 (Currently Amended): The device according to claim ~~1~~2, further comprising:

a precharge circuit connected to the bit lines of the memory cell array, the precharge circuit precharging the bit lines in response to the precharge signal.

Claim 4 (Currently Amended): The device according to claim ~~1~~2, wherein the memory cell array constitutes a DRAM.

Claim 5 (original): ~~The device according to claim 1, further~~
A semiconductor memory device comprising:

a memory cell array having a plurality of memory cells arranged in rows and columns, and bit lines and word lines connected to the memory cells;

a command buffer circuit, which receives at least an active signal to activate

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one of the rows, and a clock signal, the command buffer circuit generating an internal precharge signal to precharge the bit lines based on the active signal;

a detection circuit which monitors a potential of a word line, and detects a precharge period of said word line; and

a logic circuit which activates a word line of the word lines, in response to the active signal and a detection output signal of the detection circuit.

Claim 6 (original): A semiconductor memory device comprising:

a memory cell array having a plurality of memory cells arranged in rows and columns, and bit lines and word lines connected to the memory cells;

a command buffer circuit, which receives at least an active signal to activate one of the rows, and a clock signal, the command buffer circuit generating an internal active signal based on the active signal; and

a control circuit which generates an internal precharge signal to precharge the bit lines in response to the active signal outputted from the command buffer circuit, the control circuit controls a time in which one of the word lines is kept selected;

wherein the command buffer circuit further includes:

a latch circuit to which the clock signal and the active signal are supplied, the latch circuit latching the active signal in response to the clock signal;

a logic circuit to which the active signal latched by the latch circuit and the clock signal are supplied, the logic circuit generating the internal precharge signal; and

a delay circuit which delays the internal precharge signal supplied from the logic circuit, and generates an internal active signal.

Claim 7 (original): The device according to claim 6, the control circuit comprising:

a counter which counts the clock signal in response to the active signal, the counter outputs a signal when it counts the clock signal to a preset value;

a flip-flop circuit which is reset in response to the active signal, and set in response to the signal outputted from the counter; and

a generating circuit which generates the internal precharge signal when the flip-flop circuit is set.

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Claim 8 (Cancelled)

Claim 9 (original): The device according to claim 6, further comprising:

a precharge circuit connected to the bit lines of the memory cell array, the precharge circuit precharging the bit lines in response to the precharge signal.

Claim 10 (original): The device according to claim 6, wherein the memory cell array constitutes a DRAM.

Claim 11 (original): The device according to claim 6, further comprising:

a detection circuit which monitors a potential of a word line, and detects a precharge period of said word line; and
a logic circuit which activates a word line of the word lines, in response to the active signal and a detection output signal of the detection circuit.